ERASE INHIBIT IN NON-VOLATILE MEMORIES

ABSTRACT OF THE DISCLOSURE

The present invention presents a non-volatile memory and method for its operation that can reduce the amount of disturb in non-selected cells during an erase process. For a set of storage elements formed over a common well structure, all word-lines are initially charged with the same high voltage erase signal that charges the well to insure there is no net voltage difference between the well and word-lines. The selected word-lines are then discharged to ground while the non-selected word-lines and the well are maintained at the high voltage. According to another aspect of the present invention, this can be accomplished without increasing any pitch area circuit or adding new wires in the memory array, and at minimal additional peripheral area. Advantages include less potential erase disturb in the non-selected storage elements and a tighter erase distribution for the selected elements.